

AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning at page 2, line 22 as follows:

The MirrorBit Flash memory cell has a semiconductor substrate with implanted conductive bitlines. A ~~multiplayer~~ multilayer storage layer, referred to as a "charge-trapping dielectric layer", is formed over the semiconductor substrate. The charge-trapping dielectric layer can generally be composed of three separate layers: a tunneling layer, a charge-trapping layer, and a second insulating layer. Wordlines are formed over the charge-trapping dielectric layer perpendicular in the bitlines. Programming circuitry controls two bits per cell by applying a signal to the wordline, which acts as a control gate, and changing bitline connections such that one bit is stored by source and drain being connected in one arrangement and a complementary bit is stored by the source and drain being interchanged in another arrangement.

Please amend the paragraph beginning at page 19, line 21 as follows:

In another embodiment, as illustrated in FIG. 12, a semiconductor device ~~240~~ 510 includes a semiconductor substrate ~~242~~ 512, including buried bitlines ~~244~~ 514 and adjacent doped regions ~~246~~ 516. The semiconductor device ~~240~~ 510 also includes a second insulating layer ~~248~~ 548, i.e., insulating structures ~~248a~~ 548a, patterned to partially isolate the non-volatile memory cells. The semiconductor device ~~240~~ 510 does not include portions of a liner layer 130 interposed between the dielectric layer ~~248~~ 518 and the second insulating layer ~~248~~ 548.

Please amend the paragraph beginning at page 20, line 12 as follows:

In this embodiment, the second conductive layer 419 functions as the charge trapping layer. Additionally, the dielectric layer 418 functions as an intergate dielectric

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layer. The dielectric layer 418 may comprise a single layer or multiple layers, such as the illustrated layers 422, 424 and 426. Further, the intergate dielectric layer 418 may be of conventional dielectric material or of a high-K material as further described above. The intergate dielectric layer 418 may have a thickness of between about 1 nm and about 500 nm.